DETAILED ACTION

PRESECUTION REOPENED

1. This office action is in response to the Board of Patent Appeals and Interferences decision of August 4, 2009. Pursuant to the decision, the 35 U.S.C. §103(a) rejections over He in view of Chen and Rhodes are withdrawn. However, in view of the newly found prior art to Kozuka US 2002/0063199, PROSECUTION IS HEREBY REOPENED. A new non-final rejection is set forth below.

Claim Objections

1. Claims 1-7 and 16 are objected to because of the following informalities:

Claim 1 recites the limitation "the active region" in 12. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The specification does not provide antecedent basis for the limitation in claim 1, lines 8-9, "the local interconnect is located on the substrate between the photodiode sensing region and the reset transistor. Correction is requested.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Kozuka (2002/0063199).

As for claim 1, Kozuka shows in Figs. 1, 4 and related text a complementary metal oxide semiconductor (CMOS) image sensor device comprising:

a substrate 10;

an isolation structure 17 formed on the substrate;

a photodiode sensing region 13 formed under the isolation structure in the substrate;

a reset transistor 103 located on the substrate, wherein the reset transistor has a source region (electrically) connected to a part of the photodiode sensing region; and

a local interconnect (wire 24 combined with the gate of the source follower transistor 102 in Figure 1), wherein a first end of the local interconnect is located on the substrate between the photodiode sensing region and the reset structure, extending to an upper portion of the isolation structure to cover a periphery of the isolation structure over the photosensing region (Fig. 4) and electrically connect to the source region of the reset transistor, and a second end of the local interconnect is located on the active region of the substrate to be used as a gate of a source follower transistor 102.

As for claim 2, Kozuka shows the photodiode sensing region is located under the isolation structure.

As for claim 6, Kozuka shows the substrate is a first type conductivity P substrate and the photodiode sensing region comprises a second type conductivity N doped region.

As for claim 7, Kozuka shows the substrate is a P type substrate; and photodiode sensing region comprises a deep N well.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kozuka (2002/0063199) in view of Rhodes (6,740,915).

Kozuka disclosed substantially the entire claimed invention, as applied to claim 1 above, except a spacer is formed on a sidewall of the local interconnect.

Rhodes teaches in fig. 16 and related text a spacer 349 is formed on a sidewall of the local interconnect 342/339.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a spacer on a sidewall of the local interconnect, as taught by

Rhodes, in Kozuka's device, in order to protect the sidewalls of the interconnection and improve the performance of the device.

6. Claims 4, 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozuka (2002/0063199) in view of Chen et al. (6,392,263).

As for claims 4 and 16, Kozuka disclosed substantially the entire claimed invention, as applied to claim 1 above, including the photodiode sensing region further comprises a doped region with an N-type conductivity.

Kozuka does not explicitly disclose that the source region is an n-type doped region, such that the doped region 15 has the same as that of the source region of the reset transistor.

Chen et al. teach in Fig. 1 and related text source region 221 is an n-type doped region.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form an N-type source region, as taught by Chen et al., in Kozuka's device, in order to use the device in an application which requires an N-type transistor.

The combined device shows the source region is an n-type doped region and the photodiode sensing region further comprises a doped region with a conductivity same as that of the source region of the reset transistor, as claimed.

As for claim 5, Kozuka disclosed substantially the entire claimed invention, as applied to claim 1 above, including a P type well formed in the substrate.

Kozuka does not explicitly disclose the P type well 106 is further formed under the reset transistor.

Chen et al. teach in Fig. 4 and related text a P type well 404 is further formed under the reset transistor RS.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the P type well of the Kozuka's device, under the reset transistor, as taught by Chen et al., in order to reduce the size of the device.

Therefore, the prior art combined device shows a P type well is further formed under the reset transistor, as claimed.

Response to Arguments

7. Applicant's arguments with respect to claims 1-7 and 16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MEIYA LI whose telephone number is (571)270-1572. The examiner can normally be reached on Monday-Friday 7:30AM-5:00PM Eastern Standard Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. L./
Examiner, Art Unit 2811
12/16/2009

The reopening of prosecution after decision by the Board of Patent Appeals and Interferences is approved by:

/Gladys JP Corcoran/
Gladys Corcoran, Acting Director
Technology Center 2800
Semiconductors, Electrical and Optical Systems and Components